Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A differential amplifier circuit comprising:

a low gain fully differential amplifier; and

a high gain fully differential amplifier connected in parallel with the low gain fully differential amplifier with a positive input of the low gain fully differential amplifier being connected to a positive input of the high gain fully differential amplifier and connected to a positive input of the circuit, with a negative input of the low gain fully differential amplifier being connected to a negative input of the high gain fully differential amplifier and connected to a negative input of the circuit, negative and positive outputs of the low gain fully differential amplifier being connected to positive and negative load terminals, respectively, of the high gain fully differential amplifier,

wherein negative and positive outputs of the high gain fully differential amplifier become negative and positive outputs, respectively, of the circuit, and

wherein when the low gain fully differential amplifier biases[[,]] the high gain fully differential amplifier, the positive and negative outputs of the circuit are stable during a common mode operation without being impacted by a fluctuation of the inputs.

2. (Original): The amplifier of claim 1 wherein the low gain fully differential amplifier further includes:

at least one current source coupled to first and second differential current paths for receiving the positive and negative inputs;

a first self-biased loading in the first current path controlled by the positive input for generating the negative output thereof as a first loading bias input of the high gain differential amplifier for generating the positive output of the circuit; and

a second self-biased loading in the second current path controlled by the negative input for generating the positive output thereof as a second loading bias input of the high gain differential amplifier for generating the negative output of the circuit.

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3. (Original): The amplifier of claim 2 wherein the positive and negative inputs control the current paths by controlling gates of two pMOS transistors in the current paths.

4. (Original): The amplifier of claim 2 wherein the current source is a pMOS transistor connected to a supply voltage.

5. (Original): The amplifier of claim 2 wherein the low gain fully differential amplifier further includes a supplemental loading module for diverting current coming into the first and second differential current paths.

6. (Original): The amplifier of claim 5 wherein the supplemental loading module is an output level modification module with a current mirror type circuit sharing the current source with the two differential current paths for modifying levels of the positive and negative outputs.

7. (Original): The amplifier of claim 6 wherein the output level modification module has two nMOS transistors connected in parallel whose drains are connected to the current source.

8. (Original): The amplifier of claim 5 wherein the supplemental loading module is a gain improvement module for increasing the gain of the positive and negative outputs.

9. (Original): The amplifier of claim 8 wherein the gain improvement module has first and second nMOS transistors cross connected with each gate connected to the other's drain for sharing the current in the two differential current paths.

10. (Original): The amplifier of claim 1 wherein the high gain fully amplifier further includes:

at least one current source passing current along first and second differential current paths,

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wherein the first differential current path having a first pMOS transistor with its gate controlled by the positive input and a first nMOS transistor connected in series with a gate thereof connected to the positive output of the low gain fully differential amplifier, and the second differential current path having a second pMOS transistor with its gate controlled by the negative input and a second nMOS transistor connected in series with a gate thereof connected to the negative output of the low gain fully differential amplifier,

wherein a drain of the second nMOS transistor generates the positive output of the circuit and a drain of the first nMOS transistor generates the negative output of the circuit.

11. (Original): The amplifier of claim 1 further comprising first and second output stage modules for the positive and negative outputs of the circuit for increasing an output swing and loading capacity.

12. (Currently amended): The amplifier of claim 11 wherein each of the first and second output stage modules ~~each~~ has a pMOS transistor connected to a high voltage supply with its gate controlled by a bias voltage, an nMOS transistor connected in series with the pMOS transistor with its gate controlled by the corresponding positive or negative output of the circuit, and a capacitor providing an AC coupling to pass the corresponding positive or negative output.

13. (Original): The amplifier of claim 1 wherein the low and high gain fully differential amplifiers share at least one current source coupled to first and second differential current paths of both the low and high gain fully differential amplifiers.

14. (Original): The amplifier of claim 13 wherein the low gain fully differential amplifier further includes:

a first self-biased loading in the first current path controlled by the positive input for generating the negative output thereof as a first loading bias input of the high gain differential amplifier for generating the positive output of the circuit; and

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a second self-biased loading in the second current path controlled by the negative input for generating the positive output thereof as a second loading bias input of the high gain differential amplifier for generating the negative output of the circuit.

15. (Original): The amplifier of claim 13 wherein the positive and negative inputs control the current paths by controlling gates of two pMOS transistors in the current paths.

16. (Original): The amplifier of claim 13 wherein the low gain fully differential amplifier further includes a supplemental loading module for diverting current coming into the first and second differential current paths.

17. (Original): The amplifier of claim 13 wherein the first differential current path in the high gain fully amplifier has a first pMOS transistor with its gate controlled by the positive input and a first nMOS transistor connected in series with a gate thereof connected to the positive output of the low gain fully differential amplifier, and wherein the second differential current path has a second pMOS transistor with its gate controlled by the negative input and a second nMOS transistor connected in series with a gate thereof connected to the negative output of the low gain fully differential amplifier,

wherein a drain of the second nMOS transistor generates the positive output of the circuit and a drain of the first nMOS transistor generates the negative output of the circuit.

18. (Original): The amplifier of claim 13 further comprising first and second output stage modules for the positive and negative outputs of the circuit for increasing an output swing and loading capacity.

Claims 19-38 (Canceled).

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